CLAIMS

WHAT IS CLAIMED IS:

1. A high electron mobility transistor (HEMT) comprising:

a channel layer being composed of a II-VI compound semiconductor zinc oxide;

a gate electrode disposed on said channel layer; and

a gate insulating film disposed between said gate electrode and said channel layer and composed of at least one of a Group-III nitride compound semiconductor and a magnesium zinc oxide (MgZnO) quantum well structure.

2. A HEMT according to claim 1 wherein said gate insulating film is composed of at least one of an epitaxially grown Group-III nitride compound semiconductor and a MgZnO quantum well structure.

3. A HEMT according to claim 2 wherein said channel layer is composed of an epitaxially grown Group-II-VI zinc oxide compound semiconductor.

4. A HEMT according to claim 1 wherein said gate insulating film is composed of a Group-III compound semiconductor expressed by a chemical formula $Al_x Ga_{1-x} N$ ($0.3<x\leq 1$) or $Mg_x Zn_{1-x} O$ ($0.1<x.<.4$).

5. A HEMT according to claim 1 wherein said substrate comprises at least one of zinc oxide (ZnO), silicon carbide (SiC), sapphire (Al_2O_3), and silicon (Si) and has a bulk resistivity higher than 10^5 ohm-centimeter (Ω-cm).

6. A HEMT according to claim 1 wherein the thickness of said gate insulating film ranges from 0.30 nanometer (nm) to 50 nm.

7. A HEMT according to claim 1 employs piezoelectric doping that produces a two-dimensional electron gas (2DEG) near the interface avoiding the usage of a conventional doping method.

8. A HEMT according to claim 1 wherein said gate contact is a rectifying contact selected from the group consisting of titanium (Ti), platinum (Pt), silver (Ag), gold (Au), chromium (Cr), alloys of titanium(Ti) and tungsten (W), and platinum silicide (PtSi).

9. A HEMT according to claim 1 wherein said source and drain contacts comprise an alloy of titanium (Ti), silicon (Si), aluminum (Al) and nickel (Ni).

10. A HEMT according to claim 1 and further comprising a passivation layer on said gate and said rectifying contacts and on said heterojunction.

11. A HEMT according to claim 1 wherein said gate electrode has side walls on the lateral surfaces thereof.

12. A HEMT according to claim 1 wherein the contact area of said gate electrode with said gate-insulating film is decreased due to the presence of said sidewalls.

13. A HEMT according to claim 1 wherein the a channel layer is composed of ZnO and is grown by MOCVD.

14. A HEMT according to claim 1 wherein gate insulating film is grown by metal organic chemical vapor deposition (MOCVD) and sequentially laminated on a ZnO channel, and the ZnO channel in turn is laminated onto a ZnO substrate.

15. A HEMT according to claim 14 wherein the ZnO substrate is a c-surface substrate.

16. A HEMT according to claim 1 wherein, after the gate-insulating-film forming layer is formed on the channel layer, the dummy gate is formed, and the side walls are made on the lateral surfaces of the dummy gate, and the gate-insulating-film-forming layer is then selectively removed by using the dummy gate and the sidewalls as a mask, thereby forming a gate insulating film.

17. A method comprising:

defining a channel layer composed of a II-VI compound semiconductor zinc oxide;

forming a gate electrode disposed on said channel layer; and

forming a gate insulating film disposed between said gate electrode and said channel layer and composed of at least one of a Group-III nitride compound semiconductor and a magnesium zinc oxide (MgZnO) quantum well structure.

18. A method according to claim 17 wherein the gate insulating film is formed by metal organic chemical vapor deposition (MOCVD).

19. A method according to claim 17 wherein the ZnO substrate is a c-surface substrate.

20. A method according to claim 17 wherein, after the gate-insulating-film forming layer is formed on the channel layer, a dummy gate is formed, and side walls are made on the lateral surfaces of the dummy gate, and the gate-insulating-film-forming layer is then selectively removed by using the dummy gate and the sidewalls as a mask, thereby forming the gate insulating film.